IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Canceled)

2. (Canceled)

3. (Previously Presented) A semiconductor memory device comprising:

a semiconductor layer formed on an insulating film;

a memory cell array including a matrix arrangement of a plurality of memory cells each made up of first and second transistors connected in series, one side of each said memory cell being connected to a bit line and the other side of each said memory cell being supplied with a reference potential;

wherein said transistors are MIS-type partially depleted transistors, and;

wherein said first and second transistors have the same conduction type, and wherein a first word line is connected to the gate of said first transistor, and a second word line of the inverse logic paired with said first word line is connected to the gate of said second transistor.

4. (Original) A semiconductor memory device according to claim 3, wherein said word line and said inverse logic word line are controlled to synchronously change in state.

5. (Original) A semiconductor memory device according to claim 3, wherein one of said first word line and said second word line change in state with a predetermined delay time after the other changes in state.

6. (Original) A semiconductor memory device according to claim 3, wherein an inverter is provided between said first word line and said second word line to invert the signal level.

7.(Original) A semiconductor memory device according to claim 3, wherein said transistors having the same conduction type are n-channel type transistors.

8. (Previously Presented) A semiconductor memory device comprising:

a semiconductor layer formed on an insulating film;

a memory cell array including a matrix arrangement of a plurality of memory cells each made up of first and second transistors connected in series, one side of each said memory cell being connected to a bit line and the other side of each said memory cell being supplied with a reference potential;

wherein said transistors are MIS-type partially depleted transistors~~, and;~~

wherein said first transistor and said second transistor are opposite in conduction type from each other, and a common word line is connected to the gates of said first transistor and said second transistor; and

wherein a connection node of said first transistor and said second transistor is in a floating state.

9. (Previously Presented) A semiconductor memory device according to claim 3, wherein each said memory cell made up of said first and second transistors is formed in a region surrounded by an element isolation region.

10. (Previously Presented) A semiconductor memory device according to claim 3, wherein said insulating film and said semiconductor layer are formed on a semiconductor substrate.

11. (Previously Presented) A semiconductor memory device according to claim 3, wherein said insulating film and said semiconductor layer are semiconductor layers on a semiconductor substrate.

12. (Previously Presented) A semiconductor memory device according to claim 9, wherein said element isolation region is a trench-type element isolation film.

13. (Canceled)

14. (Canceled)

15. (Previously Presented) A semiconductor memory device comprising:

a semiconductor layer formed on an insulating film;

a memory cell array including a matrix arrangement of a plurality of memory cells each made up of first and second transistors body regions thereof being connected in series, one side of each said memory cell being connected to a bit line and the other side of each said memory cell being supplied with a reference potential,

wherein a threshold value of one of said transistors is controlled by controlling injection or discharge of an electric charge to or from a body region of one of said transistors of a selected memory cell, thereby to store data;

wherein said transistors are MIS-type partially depleted transistors, and;

wherein injection of the electric charge into the body region of said partially-depleted transistor is affected by impact ions generated by a flow of a channel current.

16. (Withdrawn) A semiconductor memory device manufacturing method comprising:

forming an oxide layer and a silicon active layer on a semiconductor substrate;

forming an element isolation region for separating said silicon active layer into discrete element-forming regions to be substantially flush with said silicon active layer;

forming gate electrode of paired two transistors by depositing a gate electrode material on said silicon active layer and patterning it;

injecting predetermined ions into a region for forming a diffusion layer in, using said gate electrodes as an ion injection mask;

forming said paired transistors by activating the injected ions through a heat process; and

forming a first gate line connected to the gate electrode of one of said paired transistors and a second gate line connected to the gate electrode of the other of said paired transistors.

17. (Withdrawn) A semiconductor memory device manufacturing method according to claim 16, wherein said paired transistors are MIS-type partially depleted transistors.

18. (Withdrawn) A semiconductor memory device manufacturing method according to claim 16, wherein the process of forming said oxide layer and said silicon active layer on said semiconductor substrate includes;

ion injection of oxygen ions into a silicon semiconductor substrate; and

annealing said silicon semiconductor substrate.

19. (Withdrawn) A semiconductor memory device manufacturing method according to claim 16, wherein the process of forming said oxide layer and said silicon active layer on said semiconductor substrate includes bonding a silicon active layer having an oxide layer on the bottom surface thereof onto said semiconductor substrate.

20. (Withdrawn) A semiconductor memory device manufacturing method according to claim 16, wherein said silicon active layer is thinned to a predetermined thickness by etching.